REMARKS

As indicated in the Office Action dated February 20, 2003, the Examiner has held the previously filed Response to Office Action mailed on November 30, 2002 as being non-responsive in order to allow Applicants the opportunity to amend the claims within the elected species. Applicants, therefore, are re-filing an entire revised response, which includes the amendments to the specification and drawings previously submitted in the November 20, 2002 response, as well as amendments to the claims. Applicants believe that amendments to the claims now reflect only the subject matter in the elected species. Applicants respectfully request that the Examiner reinstate the examination of claims 1, 7-12, and 22.

As an initial matter, Applicants reaffirm the election to prosecute the Group I claims, *i.e.*, claims 7-12. Applicants acknowledge Examiner's consent to examine claim 22 with the elected claims. Thus, as indicated by the Examiner in the Office Action Dated September 03, 2002, claims 1, 7-12, and 22 remain pending in the present application.

The drawings are objected to as failing to comply with 37 35 C.F.R. § 1.84(p)(5) because they do not include proper reference signs mentioned in the description. The drawings have been corrected to address the Examiner's objections. Corrected drawings are attached.

The specification has been amended as suggested by the Examiner to correct typographical errors. Applicants respectfully assert that no new matter has been added as a result of the amendments to the specification. Applicants respectfully assert that the Examiner's objections to the disclosure have been addressed and as a result, the objections are moot in light of the amendments to the specification.

The Examiner rejected claims 1, 7, and 22 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,428,673 (***Ritzdorf***) considered with Wolf, *et al.* Silicon Processing for the VLSI Era, Vol. 1-Process Technology, 2nd ed., Lattice Press: Sunset Beach CA, 2000, pp. 799-800 (***Wolf***). Applicants respectfully traverse this rejection.

Applicants respectfully assert that ***Ritzdorf*** (even when considered with ***Wolf***) does not teach, disclose, or suggest all of the elements of claims 1, 7 and 22 (as amended). ***Ritzdorf*** is directed towards a system for receiving a wafer for processing, e.g., electrochemical plating. ***Ritzdorf*** discloses forming a seed layer upon a wafer, and transporting the wafer for further analysis or processing (see for example col. 9, lines 52-55, col. 10, lines 14-16). However, ***Ritzdorf*** does not disclose forming an opening upon a first dielectric layer that is formed above a first structure, upon which a copper layer is formed and controlling a parameter based upon a measured thickness, as called for by claim 1 (as modified) of the present invention.

Additionally, ***Ritzdorf***, or any other art cited in the Office Action, does not disclose averaging the thickness data from a plurality of sites on a copper layer, as called for by claims 1 and 22 (both as amended). Controlling a parameter in response to thickness data that is averaged from data relating to a plurality of positions are among the concepts that are not disclosed by ***Ritzdorf***, but are called for by claim 1 of the present invention. Additionally, adding the disclosure of the damascene process in ***Wolf*** still would not anticipate all of the elements of claim 1. ***Wolf*** describes depositing metal and dielectric layers (see 2nd paragraph, page 800 of ***Wolf***), but fails to disclose averaging the thickness data from a plurality of sites on a copper layer or modifying a parameter in response to the averaged thickness data, as called for by claims 1 and 22 (both as modified). Therefore, adding the disclosure of ***Wolf*** to the disclosure of ***Ritzdorf***

would not result in all of the elements called for by claims 1 or 22 (both as amended) of the present invention.

Furthermore, based upon at least the arguments provided above, Applicants respectfully disagree with the Examiner that some of the elements called for by claim 1 may be inherent in light of ***Wolf*** and ***Ritzdorf***, as the Examiner does not provide evidence to support such argument. In light of the arguments provided above, all of the elements of claim 1 (as amended) of the present invention is not disclosed, taught, or suggested by ***Ritzdorf*** or ***Wolf***, or their combination. Thus, claim 1, as amended, is allowable. Additionally, for at least the reasons presented above, claim 22 (as amended), which has similar "means" elements relating to the elements of claim 1, claim 22 is also allowed.

Independent claims 1 (as amended) and 22 (as amended) are allowable for at least the reasons stated above. Dependent claims 7-12, which depend from independent claim 1, are also now considered to be patentable in light of the above-presented arguments.

The Examiner rejected claims 8-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ***Ritzdorf*** in view of U.S. Patent No. 6,298,470 (***Breiner***). Applicants respectfully traverse this rejection.

As the Examiner stated, ***Ritzdorf*** does not disclose measuring a thickness at a plurality of locations. Furthermore, averaging data relating to the thickness data is not inherent in ***Ritzdorf***. Adding the teachings of ***Breiner*** to the disclosure of ***Ritzdorf*** would still not disclose all of the elements of claims 8-12 of the present invention. ***Breiner*** is directed towards extrapolating known data to a new technology to determine and improve yields. ***Breiner*** discloses using data relating to previous generation IC manufacturing technology and applying them to new

generation IC manufacturing technology (see for example, col. 2, lines 54-65, col. 13, lines 44-56). Although, ***Breiner*** makes a passing reference to a "mean" value of data points, ***Breiner*** does not disclose measuring the thickness of copper layer at a plurality of locations on the copper layer and averaging the resultant data, as called for by claims 8-12 of the present invention. ***Breiner*** provides that the wafer data may include multiple measurements of each data point, which generally implies measuring a parameter (e.g., an electrical parameter) more that once, however, ***Breiner*** does not disclose measuring the thickness at different locations on a copper layer. Therefore, even combining ***Breiner*** and ***Ritzdorf*** would not result in all of the claims called for by claims 8-12 of the present invention.

Breiner is focused upon using manufacturing data relating to previous IC manufacturing processes and applying the data to predict yields of new IC technology manufacturing. Wherein, ***Ritzdorf*** is directed towards a system for receiving a wafer for processing, e.g., performing electrochemical plating, forming a seed layer upon a wafer, and transporting the wafer for further analysis or processing, which is different from the teachings of ***Breiner***. Without improper hindsight, one with ordinary skill in the art would not combine ***Breiner*** and ***Ritzdorf*** to produce the elements called for by claims of the present invention. However, as described above, even if ***Breiner*** and ***Ritzdorf*** were combined, all of the element of claims 8-12 would not be taught, disclosed, or suggested by ***Ritzdorf***, ***Breiner***, or their combination. Therefore, claims 8-12 are allowable.

Additionally, U.S. Patent Application 5,312,532 (***Andricacos***) mentions in passing, a standard deviation of thickness on a wafer, however ***Andricacos*** fails to disclose averaging the thickness data from a plurality of sites on a copper layer and modifying a parameter in response

to the averaged thickness data, as called for by claims of the present invention (as amended). ***Andricacos*** merely mentions a standard deviation relating to thickness uniformity relating to different compartments 14a, 14b, but does not disclose the various elements (described above) of claims of the present invention (see for example col. 4, lines 15-48, col. 10, lines 19-45). Even if the disclosure of ***Andricacos*** were combined with the disclosures of ***Breiner*** and ***Ritzdorf***, all of the elements of the claims of the present invention would not be disclosed, taught, or suggest. Therefore, claims 1, 7-12, and 22 are allowable.

Reconsideration of the present application is respectfully requested.

In light of the arguments presented above, Applicants respectfully assert that claims 1, 7-12, and 22 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Date: March 20, 2003 23720 PATENT TRADEMARK OFFICE	Respectfully submitted, Jaison C. John, Reg. No. 50,737 WILLIAMS, MORGAN & AMERSON, P.C. 10333 Richmond, Suite 1100 Houston, Texas 77042 (713) 934-7000 (713) 934-7011 (facsimile) ATTORNEY FOR APPLICANT(S)

MARKED-UP SPECIFICATION

Please amend the specification on page 17, line 15 through page 18, line 3 as follows:

Generally, the photolithography tool 1004 forms a layer of photoresist on the wafer 1002. The stepper 1006 controllably exposes the layer of photoresist to a light source through a mask or reticle to produce a desired pattern in the layer of photoresist. The etcher 1007 removes those portions of layers underlying the layer of photoresist that are exposed by the patterning produced by the mask to produce openings and/or holes in a desired pattern. The thin barrier metal layer is deposited by a barrier deposition tool 1008. The electroplate tool 1009 forms a layer or film of copper on the surface of the wafer 1002, filling the openings and/or holes. The metrology tool 1010 measures select parameters of the wafer [102] 1002, such as physical characteristics and/or electrical properties. The measured physical characteristics may include thickness of the copper layer, feature sizes, depth of an etching process, etc. The measured electrical properties may include resistance, conductivity, voltage levels, etc. In some embodiments, the metrology tool 1010 may not be needed, as sufficient feedback information for controlling parameters of the tools 1004-1009 may be obtained from sensors within the tools 1004-1009.

Please amend the specification on page 22, line 24 through page 23, line 5 as follows:

The controller 1106 of the electroplate tool [1019] 1009 is coupled to the controller 1012 over the line 1019. This connection allows the controller 1012 to deliver signals that instruct the controller 1106 to vary some or all of the parameters discussed above to alter the thickness of the copper layer 640 based on data received from the metrology tool 1010. For example, if the metrology tool 1010 detects that the copper layer 640 is too thin, then the controller 1012

delivers a control signal to the controller 1106, instructing the controller 1106 to alter one or more of its parameters to increase the thickness of the copper layer 640.

Please amend the specification on page 25, line 18-25 as follows:

The present invention may be employed on a lot-by-lot basis and/or on a wafer-by-wafer basis. In general, the more frequent the measurements, the more uniform and accurate will be the electroplate process performed by the electroplate tool 1009. That is, the thickness of the copper layer 640 need not be measured on each wafer [102] 1002, but rather, a previous measurement may be used by the controller 1012 to control the parameters of the electroplate tool 1009 to produce the desired thickness of the copper layer 640. The number of wafers processed between measurements is a matter of design discretion, which depends substantially on the details of the particular embodiment.

MARKED-UP CLAIMS

1. (Amended) A method comprising:

forming a first dielectric layer above a first structure layer;

forming a first opening in the first dielectric layer;

forming a first copper layer above the first dielectric layer and in the first opening; and

measuring an actual thickness of the copper layer, measuring the actual thickness comprises averaging a plurality of thicknesses from a plurality of locations on said first copper layer;

comparing the actual thickness to a desired thickness; and

varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness.

22. (Amended) A system, comprising:

means for forming a first dielectric layer above a first structure layer;

means for forming a first opening in the first dielectric layer;

means for forming a first copper layer above the first dielectric layer and in the first opening;

means for measuring an actual thickness of the copper layer, measuring the actual thickness comprises averaging a plurality of thicknesses from a plurality of locations on said first copper layer;

means for comparing the actual thickness to a desired thickness; and

means for varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness.

MARKED-UP DRAWINGS

(Please see attached marked-up, red-lined drawing of Figure 11)

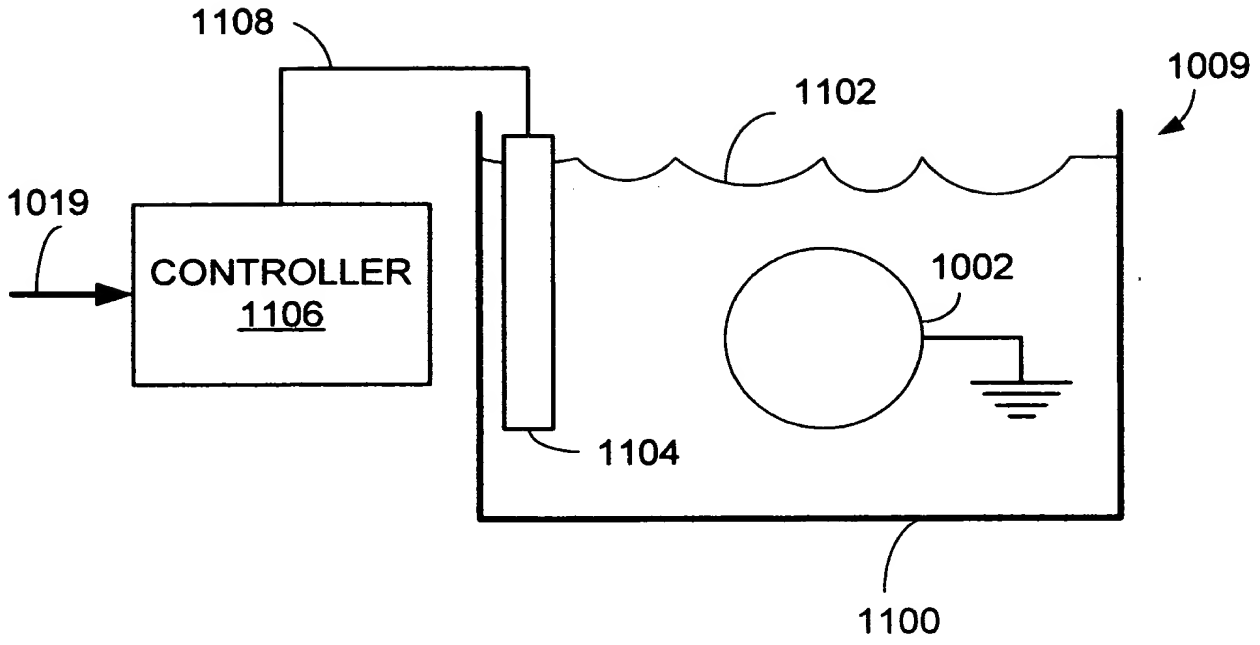

Figure 11